Amendments to the Claims

This listing of claims will replace all prior versions and listing of claims in the application:

Listing of Claims:

1. (cancelled)

2. (currently amended) An ~~The~~ integrated circuit ~~of claim 1~~ comprising:

a plurality of memory banks;

a plurality of comparator units, a comparator unit being coupled to a memory bank for comparing a test pattern written to the memory bank against data read from the memory bank; and

a BIST control unit coupled to the plurality of comparator units for testing the plurality of memory banks simultaneously, the BIST control unit provides test control signals and the test pattern to the comparator units, wherein the test control signals comprise addresses of memory words to be tested.

3. (currently amended) The integrated circuit of claim 2 wherein the memory banks occupy a common address space and the BIST control unit generates addresses in the common address space.

4. (cancelled)

5. (cancelled)

6. (currently amended) The integrated circuit of claim 5 wherein the memory banks can have different sizes.

7. (currently amended) The integrated circuit of claim ~~1~~ 2 wherein the comparator units stores faulty addresses ~~of faulty cells~~.

8. (cancelled)

9. (currently amended) The integrated circuit of claim ~~1~~ 2 wherein the BIST control unit receives test results from the comparator units.

10. (original) The integrated circuit of claim 9 wherein the BIST control unit outputs the test results serially in response to an input clock signal.

11. (original) The integrated circuit of claim 10 wherein the test results comprise addresses of faulty words.

12. (currently amended) The integrated circuit of claim ~~11~~ 10 wherein the test results ~~further~~ comprise addresses of faulty words and locations of faulty bits within the faulty words.

13. (currently amended) The integrated circuit of claim ~~1~~ 9 wherein the ~~memory bank comprises at least one memory sub-array~~ test results comprise addresses of faulty words.

14. (currently amended) The integrated circuit of claim ~~13~~ 9 wherein the ~~memory sub-array comprises a plurality of memory cells~~ test results comprise addresses of faulty words and locations of faulty bits within the faulty words.

15. (currently amended) ~~The~~ An integrated circuit ~~of claim 14~~ comprising:

a memory array having a plurality of memory banks, wherein a memory bank including a plurality of memory cells, wherein ~~the~~ a memory cell ~~comprises~~ includes a first port and a second port;

a plurality of comparator units, a comparator unit being coupled to a memory bank for comparing a test pattern written to the memory bank against data read from the memory bank; and

a BIST control unit coupled to the plurality of comparator units for testing the plurality of memory banks in parallel, the BIST control unit provides test control signals and the test pattern to the comparator units.

16. (currently amended) The integrated circuit of claim 15 wherein ~~first bit lines and second bit lines interconnect the memory cells in a first direction~~ the test mode can be either single port or dual port test mode.

17. (currently amended) The integrated circuit of claim 16 wherein ~~first word lines and second word lines interconnect the memory cells in a second direction~~ the comparator unit comprises a test control unit and a testing circuit, the test control unit is coupled to an access control circuit and a refresh control unit.

18. (currently amended) The integrated circuit of claim ~~17~~ 15 wherein ~~memory access is performed through the first port~~ the comparator unit comprises a test control unit and a testing circuit, the test control unit is coupled to an access control circuit and a refresh control unit.

19. (currently amended) The integrated circuit of claim 18 wherein ~~refresh is performed through the second port~~ the test control signals comprise addresses of memory words to be tested.

20. (currently amended) The integrated circuit of claim 19 wherein ~~memory access is performed through the second port~~ the memory banks can have different sizes.

21. (currently amended) The integrated circuit of claim 19 wherein the comparator units ~~comprises a test control unit and a testing circuit~~ store faulty addresses.

22. (currently amended) The integrated circuit of claim ~~21~~ 20 wherein the ~~test control unit is coupled to an access control circuit and a refresh control unit~~ BIST control unit receives test results from the comparator units.

23. (currently amended) The integrated circuit of claim ~~1~~ 22 wherein the ~~testing comprises single port testing~~ comparator units store faulty addresses.

24. (cancelled)

25. (new) An integrated circuit comprising:

a memory array which includes a plurality of memory banks;

a plurality of comparator units, wherein at least one comparator is associated with one memory bank, the plurality of comparators facilitate parallel testing of the memory banks simultaneously; and

a BIST control unit coupled to the memory array, the BIST control unit receives input control signals and, in response to the input control signals, causes the integrated circuit to be in test mode and generates test control signals and a test pattern, the comparator units compare the data read with the test pattern written to the memory banks.

26. (new) The integrated circuit of claim 25 wherein memory cells of the memory array comprises dual-port memory cells and the test mode can be either single port or dual port test mode.

27. (new) The integrated circuit of claim 25 wherein some or all the plurality of memory banks can be of different sizes.

28. (new) The integrated circuit of claim 27 wherein memory cells of the memory array comprise dual-port memory cells and the test mode can be either single port or dual port test mode.

29. (new) The integrated circuit of claim 25 wherein the test control signals comprise memory addresses to be tested.

30. (new) The integrated circuit of claim 29 wherein the test mode generates test patterns selected from march, checkerboard, wordline strip, blanket, or a combination thereof.

31. (new) The integrated circuit of claim 29 wherein defective addresses are stored in the comparator units.

32. (new) The integrated circuit of claim 29 wherein the BIST control unit outputs the test results comprising addresses of faulty words.

33. (new) The integrated circuit of claim 29 wherein the BIST control unit outputs the test results comprising addresses of faulty words and locations of faulty bits within the faulty words.